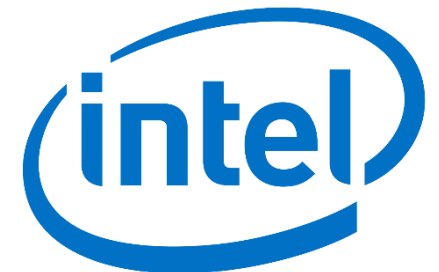


# 3<sup>rd</sup> Data Prefetching Championship

June 23<sup>rd</sup>, 2019

Held in conjunction with ISCA 2019

Seth Pugsley (Intel Labs) and Michael Ferdman (Stony Brook University)



# Welcome

- The 3<sup>rd</sup> Data Prefetching Championship
- History
  - Many microarchitecture competitions over the years
  - 1<sup>st</sup> DPC in 2009; 2<sup>nd</sup> DPC in 2015
- Motivation
  - Reducing cache misses still one of the greatest performance opportunities
  - Provide a common framework to compare everyone's best prefetching effort

# Simulation Framework

- ChampSim
  - Started life as the DPC2 simulator
  - User replaceable prefetchers, cache replacement, and branch predictors
  - Focus on ease-of-use above accuracy, performance
- 64KB/core storage budget to apportion between L1, L2, and L3
- Available tools/information
  - Physical address access stream
  - MSHR and prefetch queue occupancy
  - Program counter
    - Used by 8 submissions
  - \*NEW\* Metadata communication between cache levels' prefetchers
    - Used by 4 submissions

# Simulator Evaluation Methodology

- Single Core
  - 46 SPEC CPU 2017 traces with LLC MPKI  $\geq 1.0$ 
    - All traces treated equal; no weighting
  - Simulate 250M instructions after 50M instruction warmup
  - Thanks to Daniel Jiménez for allowing us to use his traces
- Multi Core
  - 40 secret mixes with 4 workloads each
    - Workloads randomly chosen from the above 46 SPEC CPU 2017 traces
  - Simulate 250M instructions/core after 50M instruction warmup
  - Single performance number/mix:  $\text{geomean}(\text{IPC}_0, \text{IPC}_1, \text{IPC}_2, \text{IPC}_3)$
- Final Score
  - (Geomean of all single core speedups) + (Geomean of all 4 core speedups)

# Thanks to

- Organizing Committee

- Seth Pugsley (general co-chair) (Intel)
- Alaa Alameldeen (general co-chair) (Intel)
- Michael Ferdman (program committee chair) (Stony Brook University)
- Mina Abbasi Dinani (submission chair) (Stony Brook University)

- Program Committee

- Zeshan Chishti (Intel), Paul Gratz (Texas A&M), Michael Huang (Rochester), Akanksha Jain (UT Austin), Natalie Enright Jerger (University of Toronto), Aamer Jaleel (Nvidia), Pierre Michaud (INRIA), Anant Nori (Intel), Stephen Somogyi (AMD), Carole-Jean Wu (Arizona State), Huiyang Zhou (NC State)

# Submissions

- 4 page paper
- 3 prefetcher code files (L1, L2, and L3)
- 8 papers accepted out of 14 submissions ( $8/14 = 57.1\%$ )

# Acceptance Methodology

- Paper reviews
  - 3 reviews each
- Simulator performance + paper reviews used to select papers
- 8 accepted papers include, with some overlap
  - Top 5 reviewed papers
  - Top 6 scoring prefetchers
- Presentation order does not indicate simulation performance

# Workshop Program

- Papers and code available at the DPC3 homepage
  - <https://dpc3.compas.cs.stonybrook.edu/>
- Talks have 20 minute timeslots including Q&A
- Schedule
  - 5 papers
  - Coffee break
  - 3 papers
  - Final results presentation